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10/807,499	03/24/2004	David John Butcher	550-540	4256

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
10/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/807,499	BUTCHER ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2007 and 20 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 July 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-48 have been considered. Claims 1, 13, 25, and 37 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendments as filed 05 January 2007, 18 April 2007 and 20 July 2007.

Examiner's Notes

3. The Examiner notes that claim 26 is marked as "Original", however, the original claim language was "A computer program product as..." but now reads "computer program product as...". The Examiner believes that this is a typographical error on the part of the Applicants, so has read the claim in its original form. If this change is intentional, please indicate so in the next response. Also, should something like this occur in the future, the Examiner will issue a Notice of Non-Compliance.

Drawings

4. The drawings are objected to because they contain hand-drawn and hand-written elements. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the

drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 1-48 are objected to because of the following informalities:

a. Claim 1: Please correct "...for copying...for determining at target branch address...for branching to a sub-routine..." to read --...[[for]] copying...[[for]] determining at target branch address...[[for]] branching to a sub-routine...--

b. Claims 2-12: Please correct "Apparatus as claimed..." to read --The apparatus ~~Apparatus~~ as claimed...--

c. Claim 13: Please correct "...to determine a target branch address...to branch to a sub-routine..." to read --...~~to determine~~ determining a target branch address...~~to branch~~ branching to a sub-routine...--

d. Claims 14-24: Please correct "A method as claimed..." to read --[[A]]The method as claimed...--

e. Claims 25 and 37: Please correct "A computer program product comprising a computer-readable storage medium..." to read --A computer-readable storage medium comprising a computer program product...-- in order to clarify that the computer-readable storage medium is meant as a type of hardware storing the

computer program product, such as a CD, floppy disk, main memory, etc., not a software storage type medium, such as a software database, that the current claim language insinuates with "A computer program product comprising a computer-readable storage medium...".

f. Claims 26-36 and 38-48: Please correct "A computer program product as claimed..." to read --[[A]]The computer program product as claimed...--

6. Appropriate correction is required.

Claim Rejections - 35 USC § 101

7. Claims 1-12 are rejected under 35 U.S.C. 101 because the claimed recitation of a use, without setting forth any steps involved in the process, results in an improper definition of a process, i.e., results in a claim which is not a proper process claim under 35 U.S.C. 101. See for example *Ex parte Dunki*, 153 USPQ 678 (Bd.App. 1967) and *Clinical Products, Ltd.* v. *Brenner*, 255 F. Supp. 131, 149 USPQ 475 (D.D.C. 1966).

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-12 provides for the use of a decoder for performing, copying, determining and branching, but, since the claim does not set forth any steps involved in the method/process, it is unclear what method/process applicant is intending to encompass. A claim is indefinite where it merely recites a use without any active, positive steps delimiting how this use is actually practiced.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-5, 7, 9-11, 13-17, 19, 21-23, 25-29, 31, 33-35, 37-41, 43, and 45-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizaki et al., U.S. Patent Number 6,484,314 (herein referred to as Ishizaki) in view of Hennessy and Patterson's Computer Organization and Design: The Hardware/Software Interface ©1998 (herein referred to as Hennessy).

12. Referring to claims 1, 13, 25, and 37, taking claim 1 as exemplary, Ishizaki has taught apparatus for processing data comprising:

a. Processing logic operable to perform data processing operations (Ishizaki column 6, lines 11-29; Figure 4; and Figure 5). In regards to Ishizaki, the processing logic is inherent to the CPU of Ishizaki. See FOLDOC "central processing unit" ©1998 and "arithmetic and logic unit" ©1995 for more information.

b. An instruction decoder for decoding program instructions to control said processing logic to perform data processing operations specified by said program instructions (Ishizaki column 6, lines 11-29; Figure 4; and Figure 5). In regards to Ishizaki, the processing logic is inherent to the CPU of Ishizaki. See FOLDOC "central processing unit" ©1998, "control unit" ©1995, and "machine cycle" ©1995 for more information.

c. Wherein said instruction decoder, in response to a compare and branch instruction (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; and column 2, lines 4-11), comprises a decoder for:

i. Performing a comparison between a first value stored in a first register and a second value stored in a second register (Ishizaki column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10);

ii. For determining a target branch address from a pre-programmed stored value (Ishizaki column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10); and

iii. For branching to a sub-routine at said target branch address in dependence upon a result of said comparison (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; column 2, lines 4-11; column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10).

13. Ishizaki has not explicitly taught for copying, in dependence upon a result of said comparison, a program counter value to a third register, and for determining a target branch address from said program counter value (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; column 2, lines 4-11; column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10). However, Ishizaki has taught branching on an exception and exception handling, but not the specifics on how exception handling affects the program counter. Hennessy has explicitly taught copying, in dependence upon a result of said comparison, a program counter value to a third register, and for determining a target branch address from said program counter value (Hennessy pages 411-413, section How Exceptions are Handled). In regards to Hennessy,

the program counter of the instruction causing the exception is stored in the EPC and, as Hennessy states on page 412 "The operating system knows the reason for the exception by the address at which it is initiated." This means that the address of the instruction causing the exception is needed to determine why the exception was initiated so that the proper exception handler is accessed. A person of ordinary skill in the art at the time the invention was made, and as taught by Hennessy, would have recognized that copying the program counter value and determining a target branch address from the program counter value allows the operating system to take the appropriate action to report and correct the error then restart execution of the program (Hennessy page 411). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate copying the program counter value and determining the branch target address from the program counter value to ensure the exception handler takes the appropriate action to report and correct the error and restart program execution when the exception is handled.

14. Claims 13, 25, and 37 contain similar limitations to claim 1 and are rejected for similar reasons. The claims differ from claim 1 in that claim 13 is a method and claims 25 and 37 are computer program products.

15. Regarding to claims 2, 14, 26, and 38, Ishizaki in view of Hennessy has taught, taking claim 2 as exemplary, apparatus as claimed in claim 1, wherein said instruction is an array bounds checking instruction and said sub-routine is an array bounds exception handling routine (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; column 2, lines 4-11; column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10). Claims 14, 26, and 38 contain similar limitations to claim 2 and are rejected for similar reasons.

16. Regarding claims 3, 15, 27, and 38, Ishizaki in view of Hennessy has taught, taking claim 3 as exemplary, apparatus as claimed in claim 1, wherein at least one of said first register and said second register are specified within said compare and branch instruction (Ishizaki column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10). Claims 15, 27, and 38 contain similar limitations to claim 3 and are rejected for similar reasons.

17. Regarding claims 4, 16, 28, and 40, Ishizaki has taught, taking claim 4 as exemplary, apparatus as claimed in claim 2, wherein said first value is a reference value specifying an array size and said second value is a test value determined from a decoded program instruction (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; column 2, lines 4-11; column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10). Claims 16, 28, and 40 contain similar limitations to claim 4 and are rejected for similar reasons.

18. Regarding claims 5, 17, 29, and 41, Ishizaki in view of Hennessy has taught, taking claim 5 as exemplary, apparatus as claimed in claim 4, wherein said comparison determines whether said reference value is greater than or equal to said test value (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; column 2, lines 4-11; column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10). Claims 17, 29, and 41 contain similar limitations to claim 5 and are rejected for similar reasons.

19. Regarding claims 7, 19, 31, and 43, Ishizaki has taught, taking claim 7 as exemplary, apparatus as claimed in claim 2, wherein said branching operation comprises copying a pointer to said array bounds exception handling routine into a register specifying a next program instruction (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; and column 2, lines 4-11). Claims 19, 31, and 43 contain similar limitations to claim 7 and are rejected for similar reasons.

20. Regarding claims 9, 21, 33, and 45, Ishizaki in view of Hennessy has taught, taking claim 9 as exemplary, apparatus as claimed in claim 1, wherein said compare and branch instruction is executed within a single processing cycle of said data processing apparatus when the branch is not taken (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; column 2, lines 4-11; column 4, line 48 to column 5, line 34 and column 5, line 51 to column 6, line 10). Claims 21, 33, and 48 contain similar limitations to claim 9 and are rejected for similar reasons.

21. Regarding claims 10, 22, 34, and 46, Ishizaki in view of Hennessy has taught, taking claim 10 as exemplary, apparatus as claimed in claim 1, wherein said instruction decoder is operable to decode translated platform-independent program instructions (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; and column 2, lines 4-11). Claims 22, 34, and 46 contain similar limitations to claim 10 and are rejected for similar reasons.

22. Regarding claims 11, 23, 35, and 47, Ishizaki in view of Hennessy has taught, taking claim 11 as exemplary, apparatus as claimed in claim 10, wherein said platform independent program instructions are one of:

a. Java bytecodes (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; and column 2, lines 4-11);

b. .net bytecodes;

c. MSIL bytecodes; and

d. CIL bytecodes.

23. Claims 22, 34, and 46 contain similar limitations to claim 10 and are rejected for similar reasons.

24. Claims 6, 18, 30, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizaki in view of Hennessy, as applied to claims 4, 16, 28, and 40 above, in view of "The Art of Assembly Programming" ©30 September 1996 (herein referred to as Assembly Programming). Taking claim 6 as exemplary, Ishizaki has not taught apparatus as claimed in claim 4, wherein said result of said comparison is determined from a carry flag value and zero flag value. Assembly Programming has taught wherein said result of said comparison is determined from a carry flag value and zero flag value (Assembly Programming Sections 6.5.3 and 6.9.4). Ishizaki has taught in column 5, line 17 that a greater than or equal to compare and branching instruction is performed. However, Ishizaki has not taught explicitly how the compare functions, e.g. how the results are determined, and how the compare instruction directly affects the jump function. Assembly Programming has explicitly taught a method for the compare instruction, which only sets the flags register (Assembly Programming Section 6.5.3), and that the compare instruction flag results directly influence the conditional jumps (Assembly Programming Section 6.9.4). A person of ordinary skill in the art at the time the invention was made would have recognized that the compare and jumps of Assembly Programming implements the compare and jumps without using too much memory, since it does not need to store the subtraction results. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the compare and jumps of Assembly Programming in the device of Ishizaki. Claims 18, 30, and 42 contain similar limitations to claim 6 and are rejected for similar reasons.

25. Claims 8, 20, 32, and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizaki in view of Hennessy, as applied to claims 1, 13, 25, and 37 above, in view of Schmidt et

al., U.S. Patent Number 5,727,227 (herein referred to as Schmidt). Taking claim 8 as exemplary, Ishizaki has not explicitly taught apparatus as claimed in claim 1, wherein said data processing apparatus comprises a co-processor and said pre-programmed stored value is read from a register of said co-processor. Schmidt has taught wherein said data processing apparatus comprises a co-processor and said pre-programmed stored value is read from a register of said co-processor (Schmidt column 3, line 45 to column 4, line 49; Figure 1; and Figure 3). Ishizaki has taught in column 6, lines 28-29 that a multi-CPU configuration may be used, but has not taught the specific functions of each CPU or their purpose in the system. Schmidt has explicitly taught the functions of each CPU in a multi-CPU system and their purpose in the overall system. A person of ordinary skill in the art at the time the invention was made, and as taught by Schmidt, would have recognized that the co-processor system of Schmidt reduces the amount of time needed to process interrupt/exception routines, thereby improving the speed of the system (Schmidt column 3, lines 33-43). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the co-processor of Schmidt in the device of Ishizaki to improve processor speed. Claims 20, 32, and 44 contain similar limitations to claim 8 and are rejected for similar reasons.

26. Claims 12, 24, 36, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizaki in view of Hennessy, as applied to claims 1, 13, 25, and 37 above, in view of Wikipedia term "Protected Mode" ©October 2003 (herein referred to as Wikipedia). Taking claim 9 as exemplary, Ishizaki has taught an apparatus as claimed in claim 1, said data processing apparatus remains in a user mode during execution of said compare and branch instruction (Ishizaki Abstract, lines 16-20; column 1, lines 13-42; column 2, lines 4-11; column 4, line 48 to column

5, line 34 and column 5, line 51 to column 6, line 10). Ishizaki has not taught wherein said data processing apparatus is operable in a user mode and a privileged mode. Wikipedia has taught wherein said data processing apparatus is operable in a user mode and a privileged mode (Wikipedia term "Protected mode"). A person of ordinary skill in the art at the time the invention was made would have recognized that protected mode does not allow other tasks to see the current tasks memory, thereby making multi-tasking more stable (Wikipedia term "Protected mode"). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the modes of Wikipedia in the device of Ishizaki to make the system more stable for multi-tasking. Claims 24, 36, and 48 contain similar limitations to claim 12 and are rejected for similar reasons.

Response to Arguments

27. Applicant's arguments with respect to claims 1-49 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Hamacher, Vranesic, and Zaky's Computer Organization Second Edition ©1984 has taught copying the PC as part of exception handling.

b. Hennessy and Patterson's Computer Architecture A Quantitative Approach Second Edition ©1996 and Third Edition ©2003 have taught exception handling including the step of copying the PC.

29. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

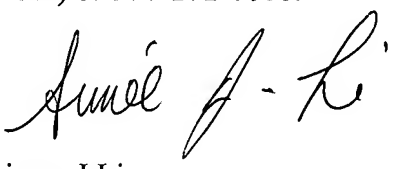
30. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

32. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

33. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Aimee J Li
Examiner
Art Unit 2183

30 September 2007